CLAIMS

1. (Amended) A semiconductor memory device comprising:

a first data holding circuit specified by driving a control line and a first data supply line;

a second holding circuit specified by driving the control line and a second data supply line and provided at a position adjacent to the first data holding circuit;

a comparison circuit for detecting an output level of the second data holding circuit and generating a timing signal in accordance with a result of comparison between this detection result and a threshold voltage; and

a drive circuit for driving the first control line in accordance with the timing signal of the comparator when reading the data from the first data holding circuit;

further comprising a control circuit for deactivating a control line by said drive circuit in accordance with a timing signal of said comparision circuit and precharging to set the bias of said second data holding circuit to a predetermined level.

2. A semiconductor memory device as set forth in claim 1, wherein said control line is a word line and said first and second data supply lines are bit lines.

3. (Deleted)

4. A semiconductor memory device as set forth in

claim 1, providing said second data holding circuit for each said first data holding circuit.

5. (Amended) A semiconductor memory device comprising:

a first data holding circuit specified by driving a first control line and a first data supply line;

a second holding circuit specified by driving a second control line and a second data supply line and provided at a position adjacent to the first data holding circuit;

a first comparison circuit for detecting an output level of the second data holding circuit and generating a timing signal in accordance with a result of comparison between this detection result and a threshold voltage;

a first drive circuit for driving the first control line in accordance with the timing signal of the first comparator when reading the data from the first data holding circuit;

a second comparison circuit for detecting the level of the second control line, comparing this detection result and the threshold voltage, and generating a second timing signal in accordance with the result; and

a second drive circuit for driving the second control line in accordance with the timing signal of the

second comparator when reading the data from the first data holding circuit,

further comprising a control circuit for deactivating a control line by said drive circuit in accordance with a timing signal of said first comparision circuit and precharging to set the bias of said second data holding circuit to a predetermined level.

6. A semiconductor memory device as set forth in claim 5, wherein said first and second control lines are word lines and said first and second data supply lines are bit lines.

7. (Deleted)

8. A semiconductor memory device as set forth in claim 5, providing said second data holding circuit in a row direction and column direction of said first data holding circuit.

9. A semiconductor memory device having:

a first memory cell connected to a word line and a pair of first bit lines,

a second memory cell connected to the word line and a pair of second bit lines, and

a word line driver activating at least the word line at a common timing and

determining the timing of the reading of the data in accordance with the level of the second bit line

connected to the second memory cell when data is read out from the first memory cell, wherein

the word line driver deactivates at least the word line connected to the second memory cell and precharges the second bit line connected to the second memory cell to the predetermined potential when the voltage difference of the pair of second bit lines becomes a previously set value.

DESCRIPTION BASED ON ARTICLE 19(1)

Claim 1 clarifies that the invention provides a comparison circuit and drive circuit, detects an output level of the second data holding circuit by the comparison circuit, compares the detection result and a threshold voltage to generate a timing signal, deactivates the control line by a drive circuit in accordance with the timing, and precharges the bias of the second data holding circuit to a predetermined level.

The citation discloses a precharge circuit, but it does not disclose a comparison circuit which detects the level of the second data holding circuit and a drive circuit which drives the control line and second data holding circuit in accordance with the timing signal of this comparison circuit.

The present invention obtains the effect that the precharge start time of the bit line of the second data holding circuit can be made earlier than the precharge start time of the bit line of the first data holding circuit and that the cycle time of the read operation can be shortened without depending on the bit line precharge of the second data holding circuit.

Claim 5 clarifies that the invention provides a second comparison circuit and second drive circuit, detects

an output level of the second data holding circuit by the second comparison circuit, compares the detection result and a threshold voltage to generate a timing signal, deactivates the control line by a second drive circuit in accordance with the timing, and precharges the bias of the second data holding circuit to a predetermined level.

The citation discloses a precharge circuit, but it does not disclose a second comparison circuit which detects the level of the second data holding circuit and a second drive circuit which drives the control line and second data holding circuit in accordance with the timing signal of this second comparison circuit.

The present invention obtains the effect that the precharge start time of the bit line of the second data holding circuit can be made earlier than the precharge start time of the bit line of the first data holding circuit and that the cycle time of the read operation can be shortened without depending on the bit line precharge of the second data holding circuit.